IN THE CLAIMS

Please amend the claims as follows:

1-5. (Cancelled)

6. (Currently Amended) A semiconductor memory comprising:

one or a plurality of processor elements having arithmetic functions;

a plurality of memory cells arranged in a matrix array;

a plurality of bit line pairs each thereof being connected to each column of the plurality of the memory cells;

a plurality of sense amplifiers of each connected to each bit line pair;

a plurality of first gate pairs;

a plurality of second gate pairs;

a plurality of first data line pairs of each to be connected with one of the bit line pairs selected via ~~by means of~~ the first gate pairs, and said first data line pairs are dedicated for a predetermined ~~specific location~~ column sub-block of the memory cells, on activation; and [[, and said plurality of processor elements are laidout to connect thereto; and]]

a plurality of second data line pairs to be connected with one of the first data line pairs via ~~by means of~~ the second gate pairs to select a predetermined ~~specific~~ row ~~location~~ of sub-block data consisting of crossbar crosspoint, [[;]] and said plurality of processor elements are connected to said plurality of second data line pairs,

wherein the first data line pair and the second data line pair are arranged to intersect each other, and said first gate pairs and said second gate pairs are adjacent to ~~arranged along the side of sub-block~~ said plurality of sense amplifiers ~~amplifier~~.

7-16. (Cancelled)